



# UNITED STATES PATENT AND TRADEMARK OFFICE

*Colin*  
UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,385	12/09/2003	Tae-Sik Oh	51345/DBP/Y35	4675
23363	7590	01/23/2006		EXAMINER
CHRISTIE, PARKER & HALE, LLP PO BOX 7068 PASADENA, CA 91109-7068				ROY, SIKHA
			ART UNIT	PAPER NUMBER
				2879

DATE MAILED: 01/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	10/731,385	OH, TAE-SIK	
	Examiner Sikha Roy	Art Unit 2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 09 December 2003.  
 2a) This action is FINAL. 2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-25 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-25 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 09 December 2003 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>12/9/03</u> .	6) <input type="checkbox"/> Other: _____.

## DETAILED ACTION

### ***Priority***

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### ***Specification***

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

### ***Claim Objections***

Claims 12 and 16 are objected to because of the following informalities:

Claim 12 line 6, 'beinginsulated' should be replaced with --being insulated --.

Claim 16 line 11 'envelop' should be --envelope--.

Appropriate corrections are required.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5,8,16-21 and 23-25 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,410,101 to Jaskie et al.

Regarding claim 1 Jaskie discloses (Figs.1,3 column 2 lines 18-34, column 3 lines 31-67) a field emission device 120 comprising a first substrate 101 and a second substrate 122 opposing one another with a predetermined gap there between, the first substrate and the second substrate being sealed, an electron emission assembly 110 formed on the first substrate and emitting electrons by generation of electric fields within electron emission assembly and an illumination assembly 100 formed on the second substrate including a transparent conductive layer 124 formed on the surface of the second substrate and having an anode input terminal to which an anode voltage 118 is applied, a phosphor screen 126 formed on the transparent conductive layer and a metal layer (reflective layer)128 formed on the screen within the vacuum assembly a portion of the metal layer 128 contacting and electrically connecting the transparent conductive layer 124. Although Jaskie does not explicitly disclose the substrates sealed by sealant forming the vacuum assembly it is inherent that field emission devices are sealed by sealant so that device is a hermetically sealed device.

Regarding claim 2 it is evident from Fig. 3 of Jaskie that the transparent conductive layer 124 and the anode input terminal connecting the anode voltage 118 are integrally formed.

Regarding claim 3 Jaskie discloses (column 2 lines 24,25) the transparent conductive layer and the anode terminal are made of indium tin oxide.

Regarding claim 4 it is evident from Fig. 3 the metal layer 128 is formed over the phosphor screen having an area larger than the phosphor screen such that the edges of the metal layer 128 contact the transparent conductive layer 124.

Regarding claim 5 Jaskie discloses (Fig. 3 column 3 lines 41-51) the electron emission assembly includes electron emission sources (emitter structure) 105 and electrodes for inducing emission of electrons from the emitters wherein the electrodes include the cathode electrodes 102 and gate electrodes 106 insulated from each other by an insulating layer 103 and formed in respective stripe patterns the cathode electrodes being substantially perpendicular to the gate electrodes.

Regarding claim 8 Jaskie discloses (Fig. 3) the cathode electrodes 102 are formed on the first substrate 101, the insulation layer 103 are formed on the first substrate covering the cathode electrodes and the gate electrodes 106(107,108) are formed on the insulation layer the insulating layer and the gate electrodes having openings for exposing the cathode electrodes and the emission sources (emitters) , the emitters being formed in the openings on the exposed cathode electrodes.

Regarding claim 16 Jaskie discloses (Fig.3) a flat panel display comprising a faceplate 100 including a faceplate interior side, a backplate 110 including a backplate interior side in an opposing relationship to the faceplate interior side, sidewalls positioned (shown one side only) between the faceplate and the backplate to form an enclosed vacuum, a phosphor layer 126 positioned on the faceplate interior side and a metal layer 128 positioned on the phosphor layer wherein the metal layer is formed within the envelope.

Regarding claim 17 it is evident from Fig. 2 that the metal layer 128 has larger area than the phosphor layer 126.

Regarding claim 18 Jaskie discloses that the metal layer contacts the electrode 124 which is connected to the anode input terminal to which anode voltage 118 is applied.

Regarding claims 19, 20 and 21 Jaskie discloses a transparent conductive layer 124 formed between the faceplate and the phosphor layer and the anode voltage is applied to this transparent conductive layer directly.

Claim 23 essentially recites the same limitations for illumination assembly of the field emission display of claim 1 and hence is rejected for the same reason. Furthermore Jaskie discloses the anode input terminal extending outside the vacuum assembly to connect to the voltage 118 and the metal layer 128 having a portion contacting and electrically connecting to the transparent conductive layer 124 within the vacuum assembly.

Claims 24 and 25 essentially recite the same limitations as of claims 2 and 4 respectively and hence are rejected for the same reasons (see rejection of claims 2 and 4).

Claims 9, 12,13 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,900,066 to Toyota et al.

Regarding claim 9 Toyota discloses (Fig. 32 column 1 lines 41-67 column 2 lines 1-10, column 27 lines 25-52) a field emission display comprising a first substrate 110 and a second substrate 30 opposing one another with a predetermined gap in between,

the first and second substrates being sealed by a sealant (bonded to each other) wherein a vacuum is formed, an electron emission assembly formed on the first substrate and emitting electrons and an illumination assembly (anode panel AP) including a phosphor screen 31 formed on the surface of the second substrate, a metal layer 33 formed on the phosphor screen within the vacuum assembly and an anode terminal extending from the vacuum assembly to outside, in which an end of the anode input terminal within the vacuum assembly contacts the metal layer 33 to be electrically connected to the metal layer.

Regarding claim 12 Toyota discloses (Fig. 32 column 1 lines 40-60) the electron emission assembly includes the electron emission sources 115A and electrodes wherein the electrodes include cathode electrodes 11 and gate electrodes 113 being insulated from each other by an insulation layer 112 and formed respectively in a stripe pattern, the cathode electrodes and gate electrodes crossing each other at right angles.

Regarding claim 13 Toyota discloses (column 20 lines 23,24 column 29 lines 50-64) the electron emission sources being carbon nanotubes, diamond.

Regarding claim 15 Toyota discloses (Fig. 32 column 1 lines 40-65) the field emission display device comprising cathode electrodes 111 formed on the first substrate 110, the insulating layer 114 formed on the first substrate covering the cathode electrodes, the gate electrodes 113 formed on the insulation layer , the insulation layer and the gate electrodes including openings for exposing the cathode electrodes and the electron emission sources 115A formed in the openings on the exposed cathode electrodes.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,410,101 to Jaskie et al. as applied to claim1 above, and further in view of U.S. Patent 6,717,340 to Nishimura.

Claim 6 differs from Jaskie in that Jaskie does not exemplify the electron emission sources (emitters) being selected from the group consisting of carbon nanotubes, graphite, diamond or combination of these materials.

Nishimura in analogous art of electron emitting devices discloses (column 3 lines 1-8) the electron emitting material selected from the group consisting of diamond-like carbon, carbon naotube, graphite. Nishimura further teaches these materials having low work function provides a device capable of driving at a low voltage.

Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to include graphite, carbon nanotubes with low work function as electron emitting material as taught by Nishimura for the emitters of Jaskie for providing a device capable of driving at a low voltage.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,410,101 to Jaskie et al. as applied to claim1 above, and further in view of U.S. Patent 5,726,530 to Peng.

Regarding claim 7 Jaskie does not disclose the gate electrodes being formed on the first substrate and the insulation layer being formed on the first substrate covering the gate electrodes.

Peng in the same field of endeavor discloses an FED comprising a substrate, a plurality of gate electrodes formed on the substrate, an insulation layer covering the gate electrodes, and a plurality of cathode electrodes over the insulating layer, and teaches this embodiment to be preferred over an FED wherein the cathode electrodes are disposed over the substrate, because the former provides a display whose resolution is not limited by the provision of individual ballast resistors for each pixel, said ballast resistors having high reliability, being capable of meeting tight tolerance, and controlling the emission current of each pixel', and further the chances of short circuiting the display and its detrimental effects are reduced (see Col. 1, lines 43-60; Col. 2, lines 47-59; and Figs. 3A, 4A, 6A, 7A and 8A).

Thus, it would have been obvious to one of ordinary skill in the art at the time of invention to provide a plurality of gate electrodes on the first substrate and insulation layer covering the gate electrodes and a plurality of cathode electrodes over the insulating layer as taught by Peng for the field emission device of Jaskie for providing a display whose resolution is not limited by the provision of individual ballast resistors for each pixel, said ballast resistors having high reliability, being capable of meeting tight

tolerance, and controlling the emission current of each pixel, and further the chances of short circuiting the display and its detrimental effects are reduced.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,900,066 to Toyota et al. and further in view of U.S. Patent 6,410,101 to Jaskie et al.

Regarding claim 10 Toyota does not disclose the anode input terminal formed of material selected from a group consisting of indium tin oxide, Ni or Cr.

Jaskie discloses (column 2 lines 24, 25) the anode input terminal integrally formed with the anode and formed of indium tin oxide. It is to be noted that this configuration provides simple manufacturing of the anode input terminal.

Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to include the anode input terminal of Toyota made of indium tin oxide same as that of the metal layer as taught by Jaskie for providing simple manufacturing of the display device.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,900,066 to Toyota et al.

Regarding claim 11 Toyota discloses the claimed invention except the metal layer covering a portion of the anode input terminal. It would have been an obvious matter of design choice to have the metal layer covering a part of the anode input terminal since the applicant has not disclosed that this configuration of the metal layer solves any stated problem or is for any particular purpose and it appears that the

invention would perform equally well with the metal layer connected to the anode input terminal as disclosed by Toyota.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,900,066 to Toyota et al. and further in view of U.S. Patent 5,726,530 to Peng.

Regarding claim 14 Toyota does not disclose the gate electrodes being formed on the first substrate and the insulation layer being formed on the first substrate covering the gate electrodes.

Peng in the same field of endeavor discloses an FED comprising a substrate, a plurality of gate electrodes formed on the substrate, an insulation layer covering the gate electrodes, and a plurality of cathode electrodes over the insulating layer, and teaches this embodiment to be preferred over an FED wherein the cathode electrodes are disposed over the substrate, because the former provides a display whose resolution is not limited by the provision of individual ballast resistors for each pixel, said ballast resistors having high reliability, being capable of meeting tight tolerance, and controlling the emission current of each pixel', and further the chances of short circuiting the display and its detrimental effects are reduced (see Col. 1, lines 43-60; Col. 2, lines 47-59; and Figs. 3A, 4A, 6A, 7A and 8A).

Thus, it would have been obvious to one of ordinary skill in the art at the time of invention to provide a plurality of gate electrodes on the first substrate and insulation layer covering the gate electrodes and a plurality of cathode electrodes over the insulating layer as taught by Peng for the field emission device of Toyota for providing a display whose resolution is not limited by the provision of individual ballast resistors for

each pixel, said ballast resistors having high reliability, being capable of meeting tight tolerance, and controlling the emission current of each pixel, and further the chances of short circuiting the display and its detrimental effects are reduced.

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,410,101 to Jaskie et al.

Regarding claim 22 Jaskie discloses the claimed invention except the anode voltage applied to the transparent conductive layer through an intermediate layer.

It would have been an obvious matter of design choice to have the anode voltage applied to the transparent conductive layer through an intermediate layer since the applicant has not disclosed that this configuration of the anode voltage connection solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with the anode voltage connected directly to the transparent conductive layer as disclosed by Jaskie.

### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Patent 5,973,452 to Bojkov et al., U.S. Patent 6,037,711 to Cathey et al. and U.S. Patent 6,633,119 to Chalamala et al. disclose field emission display device including metal layer on the anode electrode.

***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sikha Roy whose telephone number is (571) 272-2463. The examiner can normally be reached on Monday-Friday 8:00 a.m. – 4:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimeshkumar D. Patel can be reached on (571) 272-2457. The fax phone number for the organization is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sikha Roy  
Patent Examiner  
Art Unit 2879

*Karabi Guharay*  
KARABI GUHARAY  
PRIMARY EXAMINER